PN - DE10155486 A1 20030528
PD - 2003-05-28
PR - DE20011055486 20011113
OPD - 2001-11-13
TI - (A1)
Arrangement for managing of peripheral status information by a computer processor in which additional flag register positions are created that are then set to the states of peripheral status registers, thus reducing polling
AB - (A1)
Arrangement for processing state information relating to external units or peripherals connected to a computer. The arrangement comprises a processor with a flag register, a controller and at least one peripheral with its own status register. To reduce loading of the ALU, the processor flag register (11) is provided with additional bit positions that are then set to the state of the status registers (12) of peripheral devices (10). An Independent claim is made for an arrangement for processing state information relating to external units or peripherals connected to a computer in which an addition flag register is created by interrupt request register of an interrupt unit with the bit states of external status registers allocated to it.
IN - (A1 B4)
AUE VOLKER [DE]; OBERTHUER THOMAS [DE]
PA - (A1 B4)
SYSTEMONIC AG [DE]
ICO - S06F201/172; S06F201/389
EC - G06F11/30; G06F13/24
IC - (A1 B4)
G06F13/24; G06F11/30
CTNP - (A1 B4)
[ ] BORDEAUX, E., HACKER, S.: "Integrating Flash Memory in an Embedded System" Circuit Cellar Ink. April 1999 (http://www.chipcenter.com/images/ccelar/e049pdf1.pdf)
[ ] "Interrupts and Programmable Flags on the ADSP- 2185/2186" Analog Devices EE-12, 14.1.1997 (http://www.analog.com/library/applicationNotes/dsp/16_Processors/ee_12.pdf)

TI - Arrangement for managing of peripheral status information by a computer processor in which additional flag register positions are created that are then set to the states of peripheral status registers, thus reducing polling
PR - DE20011055486 20011113
PN - DE10155486 B4 20040422 DW200427 G06F13/24 000pp
- DE10155486 A1 20030528 DW200346 G06F13/24 005pp
PA - (SYST-N) SYSTEMONIC AG
IC - G06F11/30 ;G06F13/24
IN - AUE V; OBERTHUER T
AB - DE10155486 NOVELTY - Arrangement for processing state information relating to external units or peripherals connected to a computer. The arrangement comprises

cessor with a flag register, a controller and at least one peripheral with its own status register. To reduce loading of the ALU, the processor flag register (11) is provided with additional bit positions that are then set to the state of the status registers (12) of peripheral devices (10).

- DETAILED DESCRIPTION - An INDEPENDENT CLAIM is made for an arrangement for processing state information relating to external units or peripherals connected to a computer in which an addition flag register is created by interrupt request register of an interrupt unit with the bit states of external status registers allocated to it.
- USE - Arrangement for managing of peripheral status information by a computer processor.
- ADVANTAGE - Loading of the ALU is reduced by provision of additional status flags as cyclic polling or querying of peripherals is reduced.
- DESCRIPTION OF DRAWING(S) - Figure shows a computer arrangement with an extended flag register.
- control unit 2
- processing unit 3
- flag register 11
- peripheral device 10
- peripheral device status register. 12
- (Dwg.1/2)

OPD - 2001-11-13
AN - 2003-484500 [46]